What is claimed is:

1. A method for forming a semiconductor device having a trench top isolation layer, comprising the steps of:

providing a substrate having at least one trench therein;

forming a collar insulating layer over the sidewall of a lower portion of the trench;

forming a first conductive layer protruding to the collar insulating layer in the lower portion of the trench;

forming a second conductive layer overlying the first conductive layer and covering the collar insulating layer;

forming an insulating spacer over an upper portion of the sidewall of the trench and separated from the second conductive layer by a gap;

thermally oxidizing a portion of the second conductive layer to form an oxide layer thereon whereby the gap is filled;

removing the oxide layer to expose the second conductive layer;

forming a reverse T-shaped insulating layer by chemical vapor deposition to serve as the trench top isolation layer; and

removing the insulating spacer.

2. The method as claimed in claim 1, further forming a gate insulated from the substrate and overlying the reverse T-shaped insulating layer.

3. The method as claimed in claim 1, wherein the collar insulating layer is a silicon oxide layer.

4. The method as claimed in claim 1, wherein the first conductive layer is a polysilicon layer.

5. The method as claimed in claim 1, wherein the second conductive layer is a doped polysilicon layer.

6. The method as claimed in claim 1, wherein the insulating spacer is composed of a pad oxide layer and an overlying silicon nitride layer.

7. The method as claimed in claim 6, wherein the insulating spacer has a thickness of about 200~300Å.

8. The method as claimed in claim 1, wherein the gap has a width of about 50~60Å.

9. The method as claimed in claim 1, wherein the reverse T-shaped insulating layer is formed by low pressure chemical vapor deposition (LPCVD).

10. The method as claimed in claim 1, wherein the reverse T-shaped insulating layer is a tetraethyl orthosilicate (TEOS) oxide.

11. A semiconductor device having a trench top isolation layer, comprising:

a substrate having at least one trench formed therein;

a collar insulating layer disposed over a lower portion of the sidewall of the trench;

a first conductive layer disposed in the lower portion of the trench and protruding the collar insulating layer;

a second conductive layer disposed overlying the first conductive layer and covering the collar insulating layer;

a reverse T-shaped insulating layer disposed overlying the second conductive layer to serve as the trench top isolation layer; and

a gate disposed overlying the reverse T-shaped insulating layer and insulated from the substrate.

12. The semiconductor device as claimed in claim 11, wherein the collar insulating layer is a silicon oxide layer.

13. The semiconductor device as claimed in claim 11, wherein the first conductive layer is a polysilicon layer.

14. The semiconductor device claimed in claim 11, wherein the second conductive layer is a doped polysilicon layer.

15. The semiconductor device claimed in claim 11, wherein the reverse T-shaped insulating layer is a tetraethyl orthosilicate (TEOS) oxide.